REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed December 23, 2004. Upon entry of the amendments in this response, claims 26 - 45 remain pending. In particular, Applicant has amended claims 26 and 37 and added new claims 46-47. Specifically, claim 26 has been amended to recite a groove formed at top corners of said shallow trench; an active area formed between two adjacent shallow trenches in said substrate, said active area having an indium doped region that is adjacent to the groove and is formed by an angled implant of indium ions.

With respect to claim 37, that claim has been amended to recite said active area having an indium doped region that is adjacent to top corners of said shallow trenches and extends under part of the gate dielectric layer by performing an angled implant of indium ions. The aforementioned limitations can potentially mitigate the effect of a localized electric field that is induced by the gate layer in groove, thereby reducing current leakage and improving Vt roll-off. (See FIGs. 3 and 10 of the specification).

With respect to claim 46, that claim has been added to recite a first doped region having a first indium concentration adjacent to top corners of said trench isolation structure; and a second doped region having a second indium concentration at a bottom of said trench isolation structure; wherein said first indium concentration is higher than said second indium concentration. The aforementioned limitations can potentially mitigate the effect of a localized electric field that is induced by the gate layer in groove, thereby reducing current leakage and improving Vt roll-off. (See FIGs. 3, 5 and 10 of the specification).

Support for the amended limitations of claims 26 and 37 can be found, for example, in FIGs. 3 and 10, page 9, lines 16-17 and page 16, lines 2-5 in the specification. Support for the

added limitations of new claims 46-47 can be found, for example, in FIGs. 3, 5 and 10, page 9, lines 16-17, page 12, lines 10-12 and page 16, lines 2-5 in the specification. No new matter has been added. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

Rejections under 35 U.S.C. 103

The Office Action indicates claims 26 - 35 and 37 – 45 are rejected under 35 U.S.C 103(a) as being unpatentable over *Puchner* (US 6,342,429) in view of *Noble* (US 5,726,095). Additionally, the Office Action indicates that claim 36 is rejected under 35 U.S.C 103(a) as being unpatentable over *Puchner* in view of *Noble*, and further in view of *Eklund* (Publication No. 2003/0096466). Applicant respectfully traverses the rejections.

With respect to *Puchner*, *Puchner* teaches a method for forming an indium field implant at the bottom of an STI trench. By performing a vertical indium implant, indium is implanted on the surface of the trench 206. An HDPCVD oxide is deposited in the trench 206. By performing planarization, the HDPCVD oxide is partially removed to obtain an STI structure 230, with indium being vertically implanted on the STI trench surface. However, *Puchner* does not teach or reasonably suggest a groove formed at top corners of said shallow trench.

Puchner also discloses that the indium exhibits only a limited mobility and is, therefore, present to maintain a high concentration. This implies that the implanted indium is difficult to be diffused underneath the gate dielectric layer during subsequent thermal treatments.

With respect to *Noble*, *Noble* teaches a MOSFET device with a gate layer 16 and a gate oxide layer 26' being formed over an active region 12. STI structures 14 are located at both sides of the active region 12. The gate layer 16 is surrounded by tungsten metallization 18 with

windows opening to the oxide layer over the drain and source areas of active region 12. However, *Noble* also does not teach or reasonably suggest a groove formed at top corners of said shallow trench.

In this regard, Applicant has amended claim 26 to recite:

> 26. A NMOS transistor having an improved narrow width Vt roll-off, comprising:
> a substrate that includes shallow trench isolation (STI) features which are comprised of a shallow trench with sloped sidewalls and a bottom, an oxide liner formed on said shallow trench sidewalls and bottom, and an insulator layer formed on said oxide liner that fills said shallow trench and extends to a level that is above the top of said substrate, ***wherein a groove is formed at top corners of said shallow trench***;
> ***an active area formed between two adjacent shallow trenches in said substrate, said active area having an indium doped region that is adjacent to the groove and is formed by an angled implant of indium ions***;
> a gate dielectric layer formed on said active areas; and
> a patterned gate layer formed on said gate dielectric layer wherein said gate layer extends over said adjacent shallow trenches.

(*Emphasis Added*).

Applicant respectfully asserts that the cited references are deficient for the purpose of rendering claim 26 unpatentable. In particular, claim 26 because the cited references, either individually or in combination, do not teach or reasonably suggest at least the features/limitations emphasized above in claim 26. Therefore, Applicant respectfully requests that claim 26 be placed in condition for allowance. Since claims 27 – 36 are dependent claims that incorporate the limitations of claim 26, Applicant respectfully asserts that the rejection of these claims also is improper and requests that these claims be placed in condition for allowance.

With respect to claim 37, that claim has been amended to recite:

> 37. A NMOS transistor having an improved narrow width Vt roll-off, comprising:
> a substrate that includes shallow trench isolation (STI) features which are comprised of a shallow trench with sloped sidewalls and a bottom, an

oxide liner formed on said shallow trench sidewalls and bottom, and an insulator layer formed on said oxide liner that fills said shallow trench and extends to a level that is above the top of said substrate;

an active area formed between two adjacent shallow trenches in said substrate;

a gate dielectric layer formed on said active areas; and

a patterned gate layer formed on said gate dielectric layer wherein said gate layer extends over said adjacent shallow trenches;

wherein said active area having an indium doped region that is adjacent to top corners of said shallow trenches and extends under part of the gate dielectric layer by performing an angled implant of indium ions.

(*Emphasis Added*).

Applicant respectfully asserts that the cited references are deficient for the purpose of rendering claim 37 unpatentable. In particular, claim 37 because the cited references, either individually or in combination, do not teach or reasonably suggest at least the features/limitations emphasized above in claim 37. Therefore, Applicant respectfully requests that claim 26 be placed in condition for allowance. Since claims 38 - 45 are dependent claims that incorporate the limitations of claim 37, Applicant respectfully asserts that the rejection of these claims also is improper and requests that these claims be placed in condition for allowance.

Regarding new claims 46-47

Please see FIGs. 3 and 5 of the present specification. In Fig. 3, an **angled** implantation 19 of indium is performed on the top corners of the trenches 14 to form an indium doped region 20. In Fig. 5, a **vertical implantation 21 of boron or indium** is then performed to form a doped region 22 below the trenches 14. In addition, the implanted indium is difficult to be diffused during subsequent thermal treatments. Accordingly, the indium concentration adjacent to the top corners of the trenches 14 is higher than the indium concentration at the bottom of the trenches 14. It is noted that Puchner (US 6,342,429) **only** performs a **vertical** indium implantation and

results in a higher indium concentration at the bottom of the trench, **unlike** claim 46 which contemplates a first doped region having a first indium concentration adjacent to top corners of said trench isolation structure; and a second doped region having a second indium concentration at a bottom of said trench isolation structure; wherein said first indium concentration is higher than said second indium concentration.

Puchner does not anticipate claim 46 because it does not teach or suggest a first doped region having a first indium concentration adjacent to top corners of said trench isolation structure; and a second doped region having a second indium concentration at a bottom of said trench isolation structure; wherein said first indium concentration is higher than said second indium concentration. As a result, the transistor according to claim 46 and the cited reference is different.

Also, Noble (US 5,726,095) does not anticipate claim 46 because it does not teach or suggest a first doped region having a first indium concentration adjacent to top corners of said trench isolation structure; and a second doped region having a second indium concentration at a bottom of said trench isolation structure; wherein said first indium concentration is higher than said second indium concentration. As a result, the transistor according to claim 46 and the cited reference is different.

As neither of Puchner nor Noble teach or suggest all the limitations recited in new claim 46, it is applicant's belief that the claim 46 is allowable over the cited references. Since claim 47 is dependent claim that incorporate the limitations of claim 46, Applicant respectfully asserts that the rejection of these claims also is improper and requests that these claims be placed in condition for allowance.

Cited Art of Record

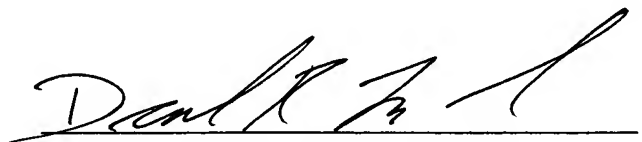
The cited art of record has been considered, but is not believed to affect the patentability of the presently pending claims.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this Amendment and Response. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

By: 

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